MICROTUNE™

TECHNICAL BACKGROUNDER: IC IMPLEMENTATION OF THE MICROTUNER™

JULY, 2000

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SHORT HISTORY OF THE TELEVISION TUNER

Television tuners, beginning with black and white TVs in the 1940s through the early color sets of the 1960s, were large electromechanical devices. These devices, which weighed about 2 pounds and were approximately the size of a cigar box, functioned as the 'tuning and receiving' component of the TV set, receiving signals from off-air broadcasts through an antenna. Both very high frequency (VHF) and ultra high frequency (UHF) bands were separated in these tuners.

In these devices, the tunable elements were manually aligned at time of manufacture. In the case of VHF, air-wound coils were gapped to alter their inductance, while for UHF, slotted disks were bent to alter their capacitance. This process was labor intensive, requiring many operators, specialized equipment and considerable factory floor space. For these reasons, during the 1960s and 1970s the manufacture of electromechanical tuners moved to countries with low labor costs. Design engineering eventually moved to be co-located with the factories.

SOLID-STATE TUNER

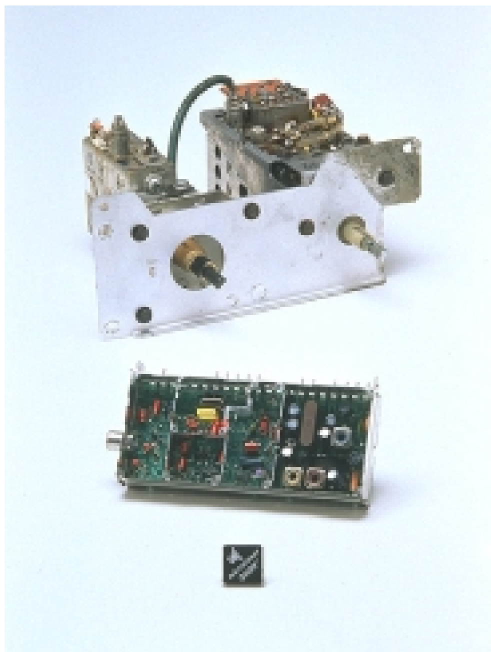
In the 1970s the solid-state tuner was introduced. It was revolutionary in its use of a synthesized, frequency-stable local oscillator, based on a quartz crystal and controlled by a microcontroller. With these features it became possible to eliminate the large knobs formerly used for changing channels, and, ultimately, enabled remote control (although many early sets that employed these tuners used push buttons on the set front for channel selection).

Despite the advances, these tuners still required air-wound coils, which in turn required hand tuning at time of manufacture. Today's solid-state tuner module uses one or two integrated circuits (ICs) and about 200 discrete components, including discrete low- noise amplifiers (LNA's), dozens of tuned coils, and several high voltage varactor diodes, mounted on both sides of a two-layer printed circuit board (PCB). The device is then completely surrounded by a full metal enclosure. The tuner has many compartments within the enclosure to provide adequate isolation between sections of circuitry. It then mounts to the television board using through-hole pins.

Today's tuner module still segments the broadband input into multiple sub-bands, often roughly corresponding with low VHF, high VHF, and UHF. The most common type of electro-mechanical tuner is the single-conversion type, used primarily for terrestrial applications like televisions and videocassette recorders. The performance of a single-conversion tuner is fundamentally determined by the electrical properties of its input tracking filters. The tracking filter circuits of the single conversion tuner use the high Q-tuned coils and varactor diodes. The tracking filters consist of a heap-shaped filter with a notch at the image frequency. Both the notch and the passband of the tracking filter must vary in frequency, with the local oscillator, so the image of the desired channel does not cause interference.

EVOLUTION OF THE TUNER

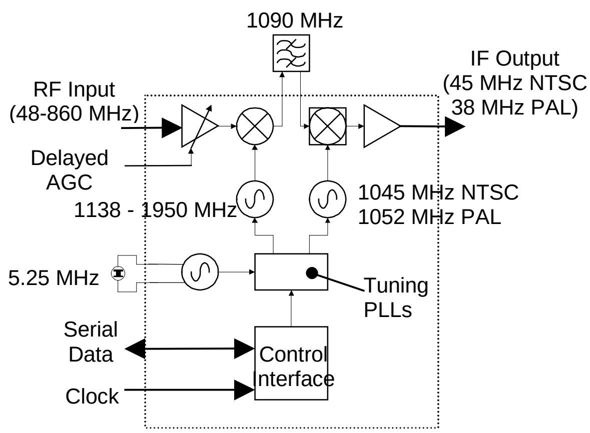
THE MECHNICAL TUNER, THE ELECTRO-MECHANICAL TUNER AND THE SINGLE-CHIP MICROTUNER



SINGLE-CHIP MICROTUNER: DESIGN OBJECTIVE

Microtune's goal was to implement a broadband RF tuner on a chip with no manually-tuned elements. In designing this IC, the engineering team considered the performance requirements of both analog (NTSC or PAL) and digital (VSB8 or QAM256), as well as, cable and terrestrial (off-air) reception. The team believed that to integrate the high Q-tuned coils was unfeasible, and in addition, did not want to complicate the fabrication process by adding high-voltage varactors. The alternative design methodology to a single-conversion tuner is the dual-conversion tuner presented below. (Figure 1).

FIGURE 1 RF TUNER ON A CHIP BLOCK DIAGRAM



A dual-conversion tuner upconverts the entire RF input to a fixed first intermediate frequency (IF) that is above the highest input frequency of interest. This allows the use of a fixed-frequency IF filter to reject the image frequencies that are created by the mixer. By first upconverting to a fixed frequency and filtering, the signals become narrowband, allowing the use of an image-reject type mixer, having very high rejection, for the downconversion. The image of the upconversion is very high in frequency and is easily 'rolled off' with a simple low-pass filter on the input, using surface mount capacitors and low-value printed inductors.

SINGLE-CHIP DUAL-CONVERSION TUNER

This chip includes the entire signal path of the dual-conversion tuner including:

- an integrated LNA with 50 dB of gain control
- an upconverting mixer
- a downconverting image reject mixer, and
- an output amplifier.

The voltage-controlled oscillators (VCOs) that drive the up converting and down converting mixers are also integrated on the IC, including the varactor diodes. The synthesizers that lock the VCOs to the reference frequency are also integrated, except for the loop filter components, which consist of very low cost, surface mounted resistors and capacitors. The active portion of the crystal oscillator is also integrated on-chip, along with a two-wire serial interface that controls the entire IC. The only external components of significance are a low-cost ceramic resonator filter at 1090 MHz and the 5.25-MegaHertz crystal. There are also a handful of surface mount devices used primarily for the bypassing power supplies.

TUNER REQUIREMENTS: DIFFERENT MARKETS DEMAND DIFFERENT PERFORMANCE PARAMETERS

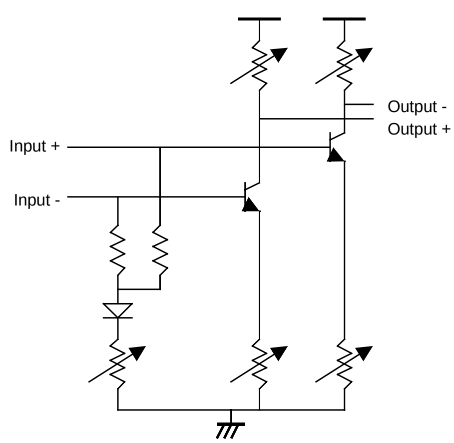
The requirements for tuners vary depending upon the market segment. The performance parameters for cable modem and cable telephony differ significantly from those of digital TV, PC/TV, and analog/digital set-top box multimedia.

Terrestrial applications, such as TV, PC/TV, and PC/DTV, are sensitive to noise figure since this determines the coverage area for the broadcaster and the ability of a given set or monitor to pull in a weak signal. Terrestrial applications also need the ability to control gain over a very large range. Analog video applications require very high linearity to avoid distortion. Digital applications require good phase noise over a range of several kHz to several MHz to avoid smearing of the dense constellation in a QAM256 application. Cable applications require a good input match over the entire band to avoid reflections and very low in band leakage, which would contaminate the cable network. Of course, all of these applications require broad RF bandwidth from 50 MegaHertz to 850 MegaHertz. This chip was designed to meet the requirements for all of these market segments and to give the broadest applicability and economy of scale

DESIGN AND MEASUREMENTS

The block that has the most impact on noise and gain control range is the LNA. A simplified schematic of this block is shown below in Figure 2.

FIGURE 2: SIMPLIFIED LNA SCHEMATIC



The LNA consists of a quasi-balanced common emitter stage with emitter degeneration. Both the emitter degeneration and load resistances are continuously variable. Initially, to reduce the gain from its maximum value, the emitter degeneration resistances are controlled. This allows the input third order intercept point to increase dB-for-dB with the gain reduction (and the output intercept to stay constant).

Additionally, the noise figure of the LNA increases at substantially less than dB-for-dB with the gain. In contrast to the use of an input attenuator, this approach allows the signal to noise ratio to increase as the input signal gets larger without degrading linearity. Once the range of resistance in the emitter degeneration has been exhausted, the load resistors are then varied. The emitter degeneration and load resistors are implemented, as shown below in Figures 3 and 4, respectively.

FIGURE 3: LNA DEGENERATION RESISTOR IMPLEMENTATION

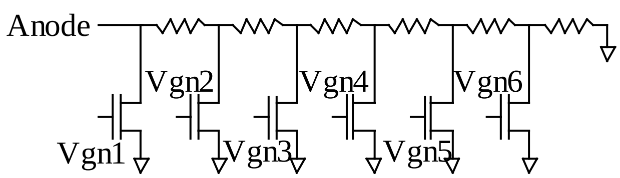
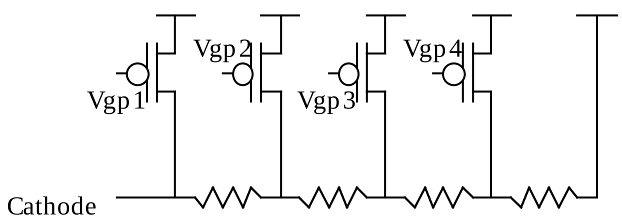


FIGURE 4: LNA LOAD RESISTOR

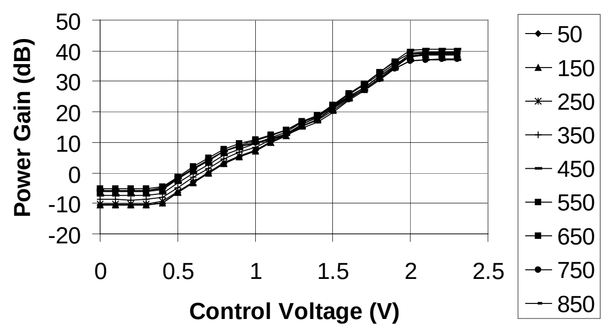


The control signals are generated in a piecewise, linear fashion to keep the NMOS and PMOS transistors in the triode region of operation for best linearity.

A plot of the power gain for the entire tuner versus delayed AGC voltage with RF input frequency as a variable parameter is shown in Figure 5. It should be noted that a 9:1 transformer is used on the output of the tuner so that a 50-Ohm spectrum analyzer can be used for this measurement. Normally, a tuner drives a SAW filter with an impedance of around 1kOhm. The transformer also reduces the apparent voltage gain by about 10 dB.

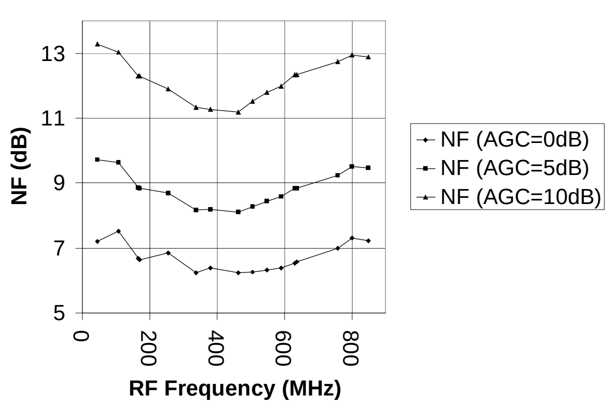
The gain slope is very linear especially at higher gain settings and lower frequencies. It can be seen from the figure that the LNA gain range is around 50 dB at low frequencies rolling off to more than 40 dB at the highest frequency. The reason for the reduced gain range at high frequency is the parasitic capacitances of the MOSFETs used in the emitter degeneration resistor network.

FIGURE 6: TUNER POWER GAIN VERSUS DELAYED AGC VOLTAGE WITH FREQUENCY AS A PARAMETER



It can also be seen that the gain variation across the band at maximum gain setting is about 3 dB. The single sideband noise figure versus RF input frequency for the entire tuner is shown in Figure 6 as a function of attenuation from maximum gain.

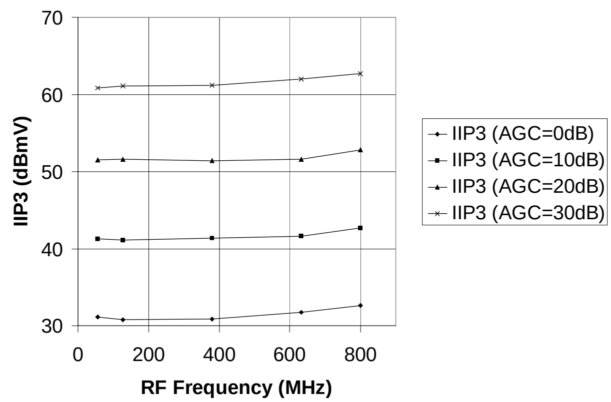
FIGURE 6: SSB NOISE FIGURE VERSUS FREQUENCY WITH ATTENUATION FROM MAXIMUM GAIN SETTING AS A PARAMETER



The noise figure is around 7 dB across the band. The overall noise figure increases about 2 dB for the first 5 dB decrease in gain and a further 3 dB for the next 5 dB decrease in gain.

The input third-order intercept for the tuner as a function of frequency with attenuation from maximum gain as a parameter is shown in Figure 7.

FIGURE 7: INPUT THIRD ORDER INTERCEPT VERSUS FREQUENCY FOR THE TUNER WITH GAIN REDUCTION AS A PARAMETER



For a given frequency the input intercept increases dB-for-dB with attenuation, as designed. It should be noted that for these measurements, two closely spaced tones (well within the 15-MHz one-dB bandwidth of the 1090-MHz filter) were used. The measured linearity is truly worst case from a practical situation, in which channels are spaced by 6-MHz or more, so that only a few channels pass through the filter. Because of this, the down-converting mixer and post amplifier dominate in the linearity measurements.

Finally, the phase noise of the tuner is critical for dense digitally modulated signals, such as 256-quadrature amplitude modulation (QAM),which is used in the most advanced cable modem designs.

Figure 8 and Figure 9, presented on the next page, show constellation diagrams for 165MHz and 723MHz desired channels in a fully loaded cable system. The desired digital channel is a 256 QAM signal with 30 dB SNR at a level of –6 dBmV. All the other channels in the fully loaded cable are analog with a carrier level of +4 dBmV.

During this test the gain level was set to maximum. The constellation diagrams are well defined, and the bit error rates (BER) are 0 (unmeasurable) when error correction is used. This shows that the tuner is suitable for even the most phase noise sensitive applications.

Figure 8: Constellation Diagram for a QAM 256 Signal at 165MHz in a Fully Loaded Cable System

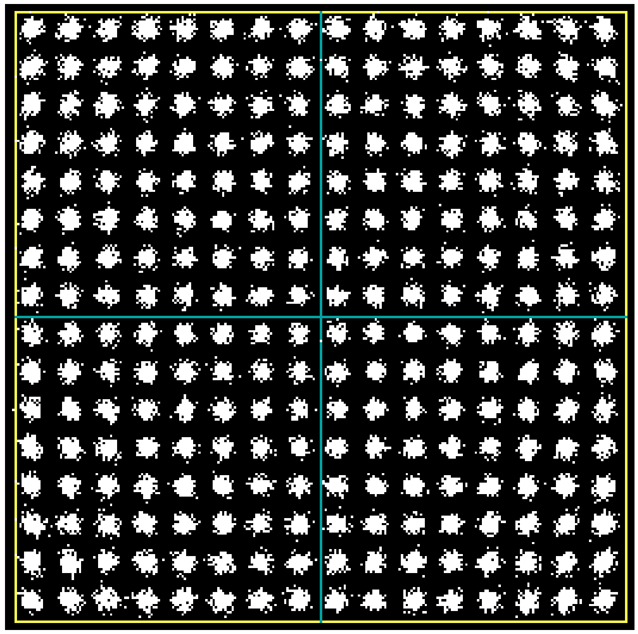
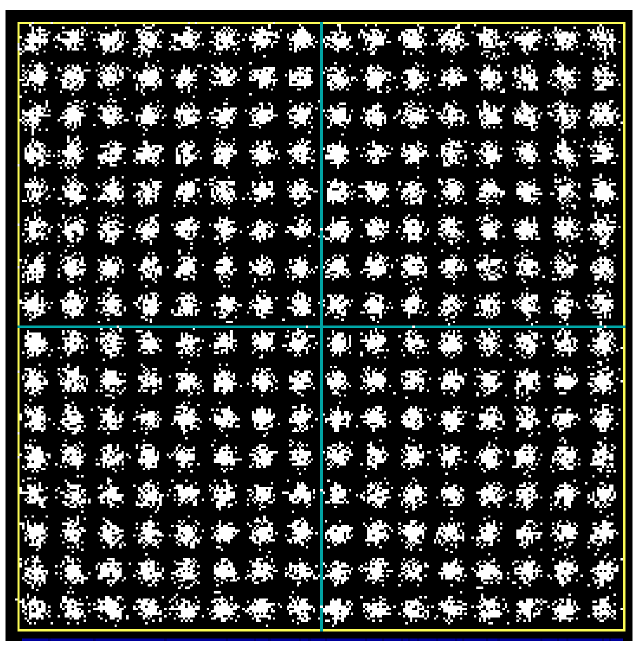


Figure 9: Constellation Diagrams for a QAM 256 Signal at 723MHz in a Fully Loaded Cable System



CONCLUSION

A single-chip RF tuner has been described and one critical block, the LNA, has been discussed in detail. Numerous important performance metrics have been shown. The tuner chip is designed for use in either a cable or terrestrial reception system, whether the signal is either digital or analog in nature.

Microtune™ implemented in a conventional, low-cost 0.8-µm BiCMOS silicon process with a peak f_τ of 12 GHz. The die size is 3.73 mm by 4.86 mm and is packaged in an 80-pin thermally enhanced TQFP. The overall phase noise for the tuner is –85 dBc/Hz at a 10-kHz offset frequency from the carrier.

The chip draws 540mA from a single 5V power supply, which is consistent with conventional dual-conversion modules. We believe that in the future it will be possible to improve performance and reduce the power consumption by 2-3 times using a more advanced BiCMOS process. It will also be possible to reduce the package pin count in future design iterations. This tuner is available today, and being designed into several applications such as PC/TV, PC/DTV, PC/VCR, analog/digital cable set top boxes.